

MANUFACTURE OF THIN FILM TRANSISTOR

Patent Number: JP63316470
Publication date: 1988-12-23
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Applicant(s): ALPS ELECTRIC CO LTD
Requested Patent: ☐ JP63316470
Application Number: JP19870152659 19870619
Priority Number(s):
IPC Classification: H01L27/12; H01L29/78
EC Classification:
Equivalents: JP2656495B2

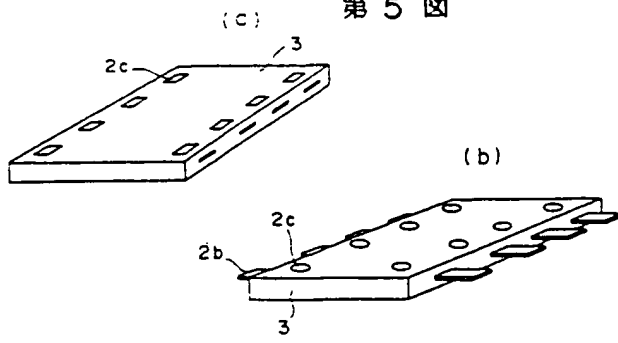
Abstract

PURPOSE: To prevent reduction clouding of ITO, by using source/drain electrodes, which are formed on an n layer, as masks and etching the n layer, and next by forming a passivation layer immediately and afterwards etching a passivation layer and a picture element at the same time.

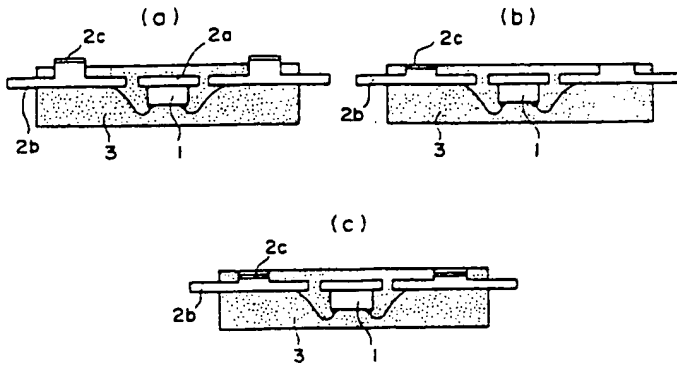
CONSTITUTION: A gate electrode 2, a picture element electrode 3 made of ITO (indium, tin oxide) materials and the like, a gate electrode layer 4, a semiconductor layer 5, and an n<+> layer 9 are formed on a substrate. A contact hole 10 is formed, and a source electrode 6 and a drain electrode 7 are formed of Al materials or the like on the n<+> layer 9. Next both these electrodes are used as masks to perform n<+> layer etching. The n<+> layer 9 is divided into two parts; a source region 5a and a drain region 5b, and a passivation layer 8 is formed thereon of silicon nitride materials or the like. Picture element etching, in which respective layers laminated on the picture element electrode 3 are removed to expose the picture element electrode 3, and passivation layer etching, in which passivation layers 8 on respective gate and source terminal parts of a thin film transistor are removed, are performed at the same time. Hence the clouding of the ITO can be prevented.

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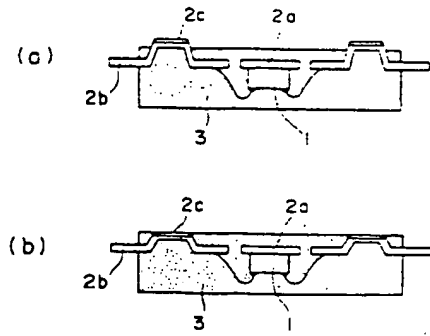
第 5 图



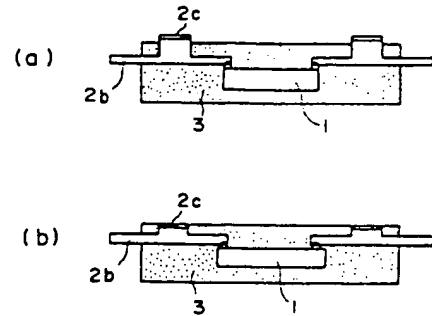
第 6 图



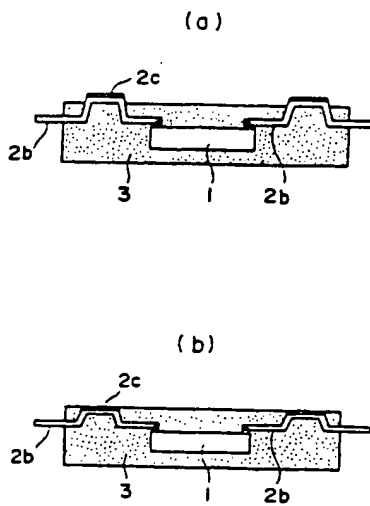
第 7 图



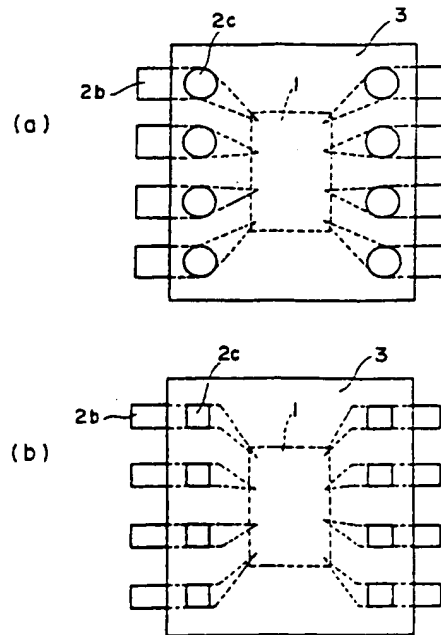
第 8 图



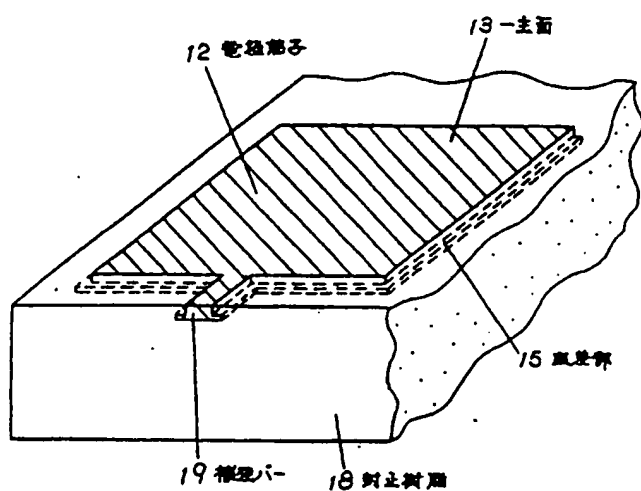
第 9 图



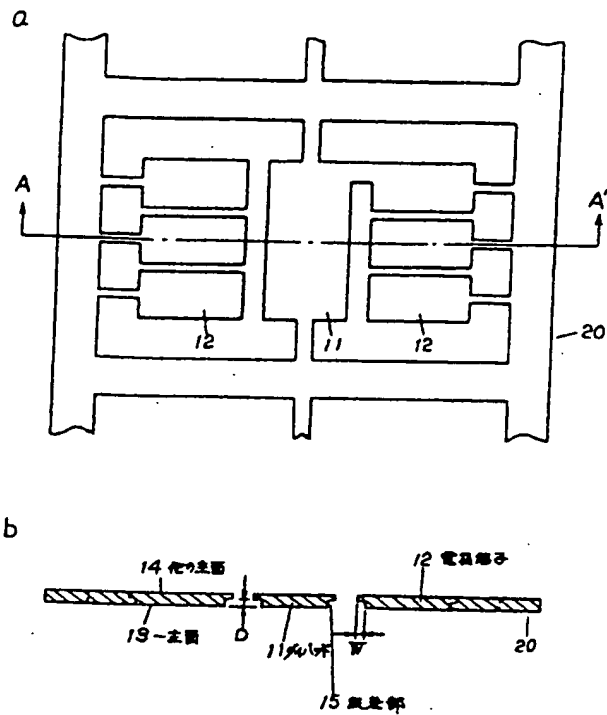
第 10 图



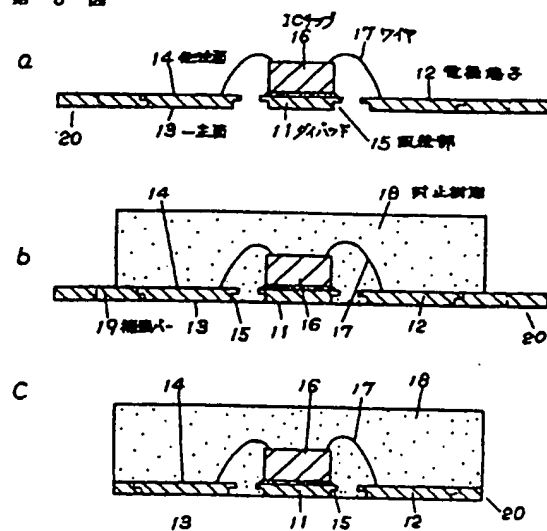
第 1 図



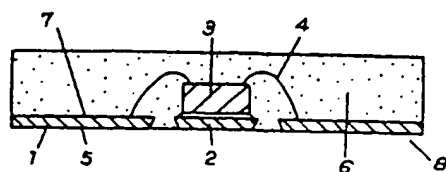
第 2 図



第 3 図



第 4 図



CLIPPEDIMAGE= JP401106456A
PAT-NO: JP401106456A
DOCUMENT-IDENTIFIER: JP 01106456 A
TITLE: SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

PUBN-DATE: April 24, 1989

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APPL-NO: JP62263435

APPL-DATE: October 19, 1987

INT-CL_(IPC): H01L023/50; H01L023/28

US-CL-CURRENT: 257/666,257/787

ABSTRACT:

PURPOSE: To make an electrode terminal not to come off due to external force and thermal strain by providing the end surface of a lead frame substrate with a stair part having more than one step and performing molding with sealing resin in a shape of covering the stair part.

CONSTITUTION: An IC chip 16 is mounted on the other main surface 14 of a die pad 11, and a pad of the IC chip and the other main surface 14 of an electrode terminal 12 are bonded with a wire 17 so as to be continuously molded with sealing resin 18 on the almost level with one main surface 13 by a transfer method so that the electrode terminal and the main surface 13 of the die pad 11 may be exposed. At this time, a stair part 15 provided on a lead frame 20 is also covered with sealing resin 18. Thereby, a reinforcing bar 19 exposed to an end surface of sealing resin 18 is also of the same projection type so as to have very strong structure against coming-off even to external force.